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Flexible MoS_2 Field-Effect Transistors for Gate-Tunable Piezoresistive Strain Sensors

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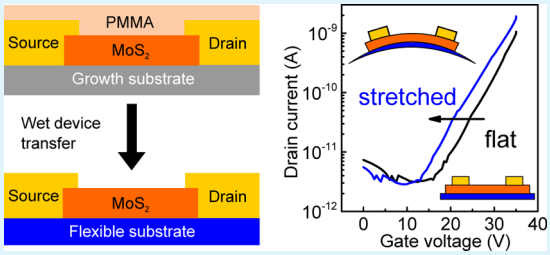
ABSTRACT: Atomically thin molybdenum disulfide (MoS_2) is a promising two-dimensional semiconductor for high-performance flexible electronics, sensors, transducers, and energy conversion. Here, piezoresistive strain sensing with flexible MoS_2 field-effect transistors (FETs) made from highly uniform large-area films is demonstrated. The origin of the piezoresistivity in MoS_2 is the strain-induced band gap change, which is confirmed by optical reflection spectroscopy. In addition, the sensitivity to strain can be tuned by more than 1 order of magnitude by adjusting the Fermi level via gate biasing.



KEYWORDS: *wafer-scale MoS_2, transition metal dichalcogenide, TMDC, field-effect transistor, flexible electronics, piezoresistive strain sensing, gauge factor*

1. INTRODUCTION

Molybdenum disulfide (MoS_2) is a layered two-dimensional (2D) semiconductor that can reach single-atomic-layer thickness by the exfoliation of natural crystals[1] or synthesis.[2−5] Atomically thin MoS_2 is promising for a number of applications[6] including field-effect transistors with high on/off ratios exceeding 10^8 and mobilities of 0.1−10 $cm^2\ V^{-1}\ s^{-1}$,[7,8] photodetectors,[8] chemical sensors,[9−12] and resonant tunneling devices.[13] Because of its superior mechanical and electrical properties and better long-term stability compared to organic semiconductors, MoS_2 is an ideal candidate for high-performance flexible and transparent electronics.[14−18] Such flexible MoS_2-based devices can offer new functionality, such as the recently observed piezoelectricity for energy conversion.[19] In addition, a wide range of devices can be realized using the piezoresistive effect typically occurring in semiconductors, including strain gauges and pressure or acceleration sensors. Even though recent spectroscopic studies and theoretical works showed that the band gap of MoS_2 can be changed under strain,[20−25] the implications of these strain-induced band gap changes on electrical devices have not been carefully explored. The work by Lee et al. has studied MoS_2 FETs under strain, but surprisingly, the authors did not observe any strain-induced changes in the electrical signal.[18] These results are in contradiction with previous optical studies and theoretical predictions.

In this work, the properties of flexible MoS_2 FETs under applied strain are investigated. It is shown that the devices are highly sensitive to strain, which is in agreement with theoretical studies and optical measurements. The origin of this effect is shown to be the strain-induced band gap change, which is confirmed by optical reflection spectroscopy. In addition, the strain sensitivity can be significantly tuned by adjusting the MoS_2 Fermi level by applying a gate bias.

2. RESULTS AND DISCUSSION

To fabricate the devices, we first grew highly uniform wafer-scale trilayer MoS_2 (approximately 2 nm thick) on a SiO_2−Si wafer according to our recently published protocol.[26] The MoS_2 transistors were fabricated using a standard UV lithography process, which includes the deposition of gold contacts and the etching of the MoS_2 channels (detailed procedure described in experimental section). As has been shown in our previous work,[26] these devices have highly reproducible electrical properties over a large area of several square centimeters across a wafer with a field-effect mobility of approximately 7 $cm^2/(V\ s)$, comparable to the exfoliated flakes of similar thickness and chemical-vapor-deposited (CVD) material. The as-fabricated MoS_2 FETs were then transferred onto a flexible polyethylene terephthalate (PET) substrate, as illustrated in Figure 1. To ensure back-gated-transistor operation, prior to the MoS_2 device transfer we coated the PET substrate with conductive indium tin oxide (ITO) as a transparent back-gate electrode and 80 nm Al_2O_3 as the gate dielectric (Figure 1). Figure 2 shows the optical images of the as-fabricated MoS_2 devices before transfer (a,b), the floating device released from the growth substrate (c), and the transferred MoS_2 devices on a flexible substrate (d,e).

Figure 3a shows the transfer curve of a representative MoS_2 FET in which the drain current (I_d) versus the back-gate voltage (V_{bg}) is measured and shown on both a linear (dashed

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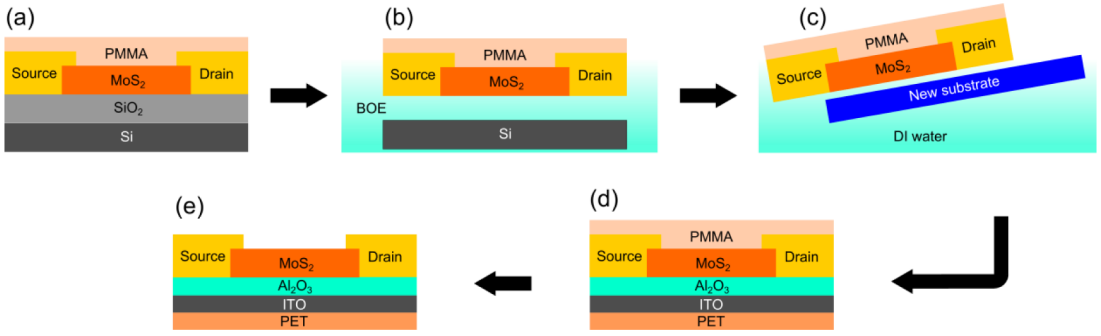

Figure 1. Fabrication of the flexible MoS_2 field-effect transistors using a device transfer technique. (a) MoS_2 field-effect transistors are fabricated on an SiO_2−Si wafer and coated with a layer of poly(methyl methacrylate) (PMMA). (b) The SiO_2 layer is chemically etched in a BOE bath to release the devices from the substrate. (c) Floating devices are held together by the PMMA layer and are transferred from a DI water bath onto a new substrate, which, in principle, can be any water-stable material. A flexible PET substrate with a conductive ITO back-gate electrode and ALD-grown Al_2O_3 dielectric is chosen here (d). (e) The PMMA layer is then removed in an acetone bath.

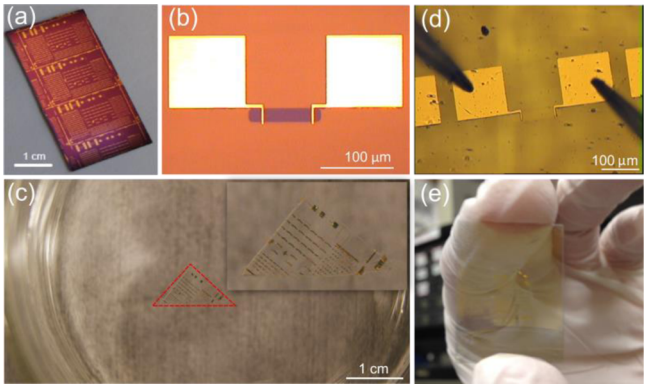

Figure 2. Optical images of the as-fabricated and flexible MoS_2 devices. (a) A top-view optical image of MoS_2 FETs after fabrication on an SiO_2−Si wafer. (b) A typical transistor with 100 μm MoS_2 channel length from the die in (a). (c) The released MoS_2 FETs held with the poly(methyl methacrylate) (PMMA) layer floating on water (the inset shows a higher magnification of the same floating sample). (d) A flexible transistor on the Al_2O_3−ITO−PET substrate with probes touching the source and drain contacts during electrical measurements. (e) Flexible MoS_2 FETs on a transparent and flexible PET substrate covered with an ITO back-gate electrode and an 80 nm Al_2O_3 dielectric layer.

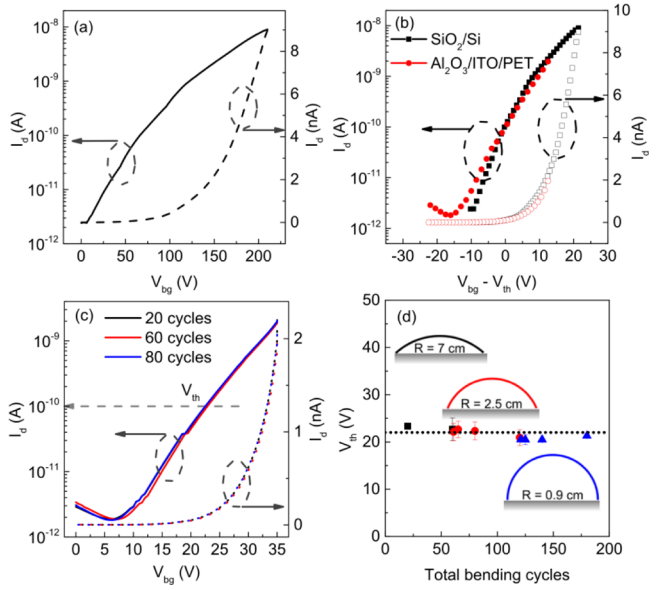

Figure 3. (a) Drain current (I_d) as a function of applied back-gate voltage (V_{bg}) of an as-fabricated MoS_2 FET (W/L = 13 μm/100 μm) on a Si substrate with a 265 nm thick SiO_2 gate dielectric, plotted on semilogarithmic scale (solid line) and linear scale (dashed line) at a constant drain-source voltage of V_{ds} = 10 V. All results shown are from the backward voltage sweeps (from high to low V_{bg}). (b) The $I_d - V_{bg}$ curves of an as-fabricated device on an SiO_2−Si wafer (squares) and of a transferred device on an Al_2O_3−ITO−PET substrate (circles) on a semilogarithmic scale (solid symbols) and linear scale (open symbols). The horizontal axis is normalized by the capacitance ratio as described in the text. (c) A representative flexible MoS_2 FET on the Al_2O_3−ITO−PET substrate measured after 20, 60, and 80 bending cycles in a vacuum (approximately 10^{-5} Torr). All curves align well on top of each other. (d) The threshold voltage (V_{th}) evolution of flexible MoS_2 FETs as a function of the total number of bending cycles. The error bars represent the results obtained with different devices. The observed device-to-device variations are small. No significant change in V_{th} is seen even after 180 bending cycles. The samples were bent around surfaces with different curvatures (bending radii r = 7 (square), 2.5 (circle), and 0.9 cm (triangle); values correspond to strain values of $\varepsilon \approx$ 0.07, 0.2, and 0.54%, respectively). All devices were measured sequentially in the flat state after a given number of bending cycles.

line) and a semilogarithmic scale (solid line). The as-fabricated MoS_2 transistors on the SiO_2/Si substrate reveal a large on−off current ratio (I_{max}/I_{min}) of ~10^4.

Figure 3b compares the electrical performance of the as-fabricated and flexible devices after transfer. Note that the applied back-gate voltages for the flexible devices are lower than those for the as-fabricated devices because the capacitance of the new gate dielectric is approximately 6.6 times larger (here we use 80 nm thick Al_2O_3 with a relative permittivity of $\varepsilon_r \approx 7.8$ instead of 265 nm thick SiO_2 with ε_r = 3.9) using the relationship as follows:

$$C_{Al_2O_3}/C_{SiO_2} = \frac{\varepsilon_{Al_2O_3}}{d_{Al_2O_3}} \Big/ \frac{\varepsilon_{SiO_2}}{d_{SiO_2}} \quad (1)$$

To make a fair comparison between the FETs on the SiO_2−/Si substrate and on the Al_2O_3−ITO−PET substrate (without any strain applied), we normalized the horizontal axis in Figure 3b by V_{th}, the thickness and the relative permittivity of the dielectric layer. Both curves show similar behavior and overlap after this normalization with minor deviations that can be attributed to differences in interface quality and surface roughness of the SiO_2−Si and the Al_2O_3−ITO−PET substrates. The results suggest that the transfer process does

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not significantly alter the device performance and therefore provides a reliable method for fabricating flexible devices.

A series of bending tests was then performed on the flexible MoS_2 transistors to investigate the influence of the number of bending cycles and the bending radius on the stability of device performance. Uniaxial strain (ε) along the longitudinal direction of the MoS_2 channel was applied by placing the sample on a rigid cylindrical surface with a well-defined curvature, and the strain was estimated using the following equation:[21] $\varepsilon = (t/r)/2$, where t is the substrate thickness (100 μm for the PET substrates used here) and r is the bending radius, which is the radius of the curved surface (a cylinder). After a specific number of bending cycles, the devices were then measured again in the flat state without strain. The I_d-V_{bg} characteristic of a representative device is plotted in Figure 3c on linear (dashed lines) and semilogarithmic scales (solid lines) as a function of the number of bending cycles (20, 60, and 80 cycles). The effect of bending on the device performance is observed to be negligible. To evaluate the influence of bending in more detail, we define the threshold voltage, V_{th}, as the applied V_{bg} value needed to achieve a drain current of $I_d = 10^{-10}$ A, i.e., the intersection between the transfer curve and the horizontal dashed line in Figure 3c. The evolution of V_{th} versus the total number of bending cycles is shown in Figure 3d for at least 5 devices (error bars) and various bending radii (r = 7, 2.5, and 0.9 cm, which correspond to the applied strain $\varepsilon \approx$ 0.07, 0.2, and 0.54%, respectively). Again, the observed variation in V_{th} is small, suggesting good mechanical stability and good device-to-device reproducibility even after more than 180 bending cycles measured over several days.

Next, the device performances under different strain conditions are compared in Figure 4. Figure 4a shows a

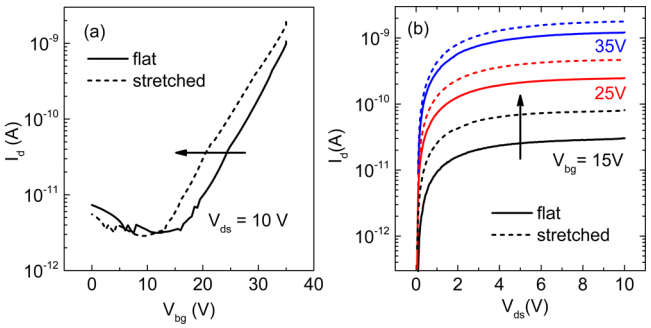

Figure 4. (a) Representative transfer curve (I_d-V_{bg}) of a flexible MoS_2 transistor measured in the flat state (solid line) and the stretched state (dashed line, applied strain ε = 0.07%). A shift of the transfer curve is observed under strain. Several devices were measured, with all showing similar behavior. (b) Output characteristic (I_d-V_{ds}) of the same device at different back-gate voltages (V_{bg}) on a semilog scale (W/L = 13 μm/100 μm).

representative transfer curve of a flexible MoS_2 transistor measured first without strain in the flat state (solid line) and afterward in a stretched state (dashed line) with an applied uniaxial strain of $\varepsilon \approx$ 0.07% along the transistor channel direction. Under strain, a shift of the entire transistor curve toward lower back-gate voltages and an electron current increase is observed, as indicated by the arrow. In addition, the output curves of the same device at different back-gate voltages (V_{bg}) are plotted on a semilog scale (Figure 4b). It is clear from Figure 4 a,b that the MoS_2 transistor is highly strain-sensitive. The resistivity change, as well as the current change, of a semiconducting material in response to the applied strain is known as the piezoresistive effect. To our knowledge, this is the first observation of the piezoresistive effect in field-effect transistors based on large-area MoS_2.

Although other effects, such as the strain-induced capacitance change of the gate dielectric, may also cause a shift of the I_d-V_{bg} curve, this capacitance-related shift is approximately 3 orders of magnitude smaller than the changes observed here[27] and is therefore neglected in the following. To confirm that the observed effect results from a band gap change, we performed reflection spectroscopy as discussed below.

Strain-induced band gap changes have been previously investigated in monolayer and bilayer MoS_2 using optical spectroscopy and simulations.[20−25] However, the effect of strain on trilayer material remains unexplored. Figure 5a shows the

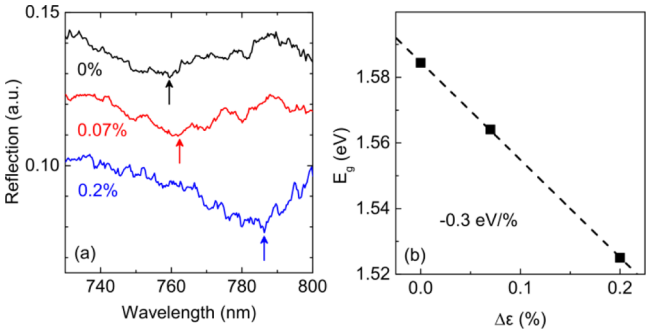

Figure 5. (a) The optical reflection spectra of trilayer MoS_2 under different applied strain values. The position of the reflection minimum shifts to a higher wavelength with increasing strain, as indicated by the arrows. The spectra are shown vertically offset for clarity. (b) Band gap E_g versus the applied strain $\Delta\varepsilon$, estimated from the minimum position in (a). The band gap linearly decreases with increasing strain. The slope is −0.3 eV per percent strain, which is in agreement with previous reports on exfoliated MoS_2.

optical reflection spectra of trilayer MoS_2 for different applied strain values. The band gap (E_g) is estimated from the wavelength (λ) of the valley position in the reflection spectrum through $E_g = 1240/\lambda$, where E_g has units of eV and λ is the wavelength in nm. A clear red shift of the reflection minimum upon an increase in strain is observed, indicating the decrease of E_g. Figure 5b shows that the extracted band gap decreases linearly with increasing strain with a slope of approximately −0.3 eV per percent strain applied, which is similar to that reported in literature.[20−25] However, the band gap change also depends on the number of MoS_2 layers due to the thickness-dependent differences in band structure. For monolayer MoS_2, the theoretically calculated band gap change lies between −0.05 and −0.085 eV per percent strain,[23,25] and the experimental results show a similar trend, with a value around −0.05 eV per percent strain.[21,25] The band gap change due to strain becomes more prominent in bilayer samples, with theoretical values ranging from −0.1 to −0.2 eV per percent strain[23,25] and experimental values around −0.12 eV.[21,24,25] The predicted theoretical value for bulk MoS_2 reaches −0.3 eV per percent strain,[22] which is very similar to the band gap change observed in the present study using trilayer MoS_2.

In addition to the strain-induced band gap change, the applied strain can affect the position of the Fermi level (φ_n) relative to the conduction band edge.[21] In a field-effect transistor, the Fermi level can also be moved with respect to the band edges of the semiconductor by utilizing chemical

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doping[28] or electrostatically by applying a gate bias. To estimate the Fermi level change, we converted the strain-induced current change ΔI to the electron concentration change (i.e., Δn) using

$$\Delta I = \mu q \Delta n \left(\frac{W}{L}\right) V_{ds} \quad (2)$$

where μ is the field-effect mobility, q is the elementary charge, W is the channel width, L is the channel length, and V_{ds} is the drain-source voltage. According to previous studies, the field-effect mobility of MoS_2 has a negligible dependence on the applied strain over a wide range (down to a bending radius of 2.2 mm).[17,29] Here, moderate strain values (≥9 mm) are applied; therefore, a constant mobility at a given V_{bg} can be assumed independent of the applied strain. The change in the electron concentration (Δn) is then estimated from ΔI and related to the Fermi level changes ($\Delta\varphi_n$) using the following expression:[30]

$$\Delta n = \left(\frac{g_c m_c^*}{\pi \hbar^2}\right) \ln\left[\exp\left(\frac{-q\Delta\varphi_n}{kT}\right) + 1\right] \quad (3)$$

where $g_c = 2$ is the degeneracy factor,[31] $m_c^* = 3.44 \times 10^{-31}$ kg is the effective electron mass,[22] $\hbar$ is the reduced Planck's constant, k is the Boltzmann constant, and T is the temperature (300 K). The estimated Fermi level change ($\Delta\varphi_n$) versus the strain ($\Delta\varepsilon$) at different applied V_{bg} values is plotted in Figure 6a. Similar to the optical reflection measurements, a linear relationship is observed between the Fermi level change relative to the conduction band edge and the applied strain. However, the slope of the linear fit depends on the gate voltage. At V_{bg} = 35 V, $\Delta\varphi_n$ decreases by approximately −0.19 eV per percent strain applied, and at V_{bg} = 15.5 V the slope becomes approximately −0.24 eV per percent strain. A negative slope means that the Fermi level moves closer to the conduction band edge. Illustrating this effect in more detail, Figure 6b shows the back-gate-voltage dependence of the Fermi level change estimated from the electrical measurements of a device under $\varepsilon \approx 0.07\%$. The right vertical axis shows $\Delta\varphi_n$ per percent strain applied. A nonmonotonic dependence of $\Delta\varphi_n$ on V_{bg} is observed, with a maximum in the subthreshold region. Because of the exponential change of I_d with V_{bg} in the subthreshold region, the relative current change (ΔI) between the stretched and the flat transistors is large, and so is the change in the carrier concentration. As a result, with increasing V_{bg} the movement of the Fermi level toward the conduction band edge in this region is abrupt, and a local maximum of $\Delta\varphi_n$ is formed near V_{th}. However, above V_{th} the Fermi level change with gate bias is weaker, causing less sensitivity to the applied strain.

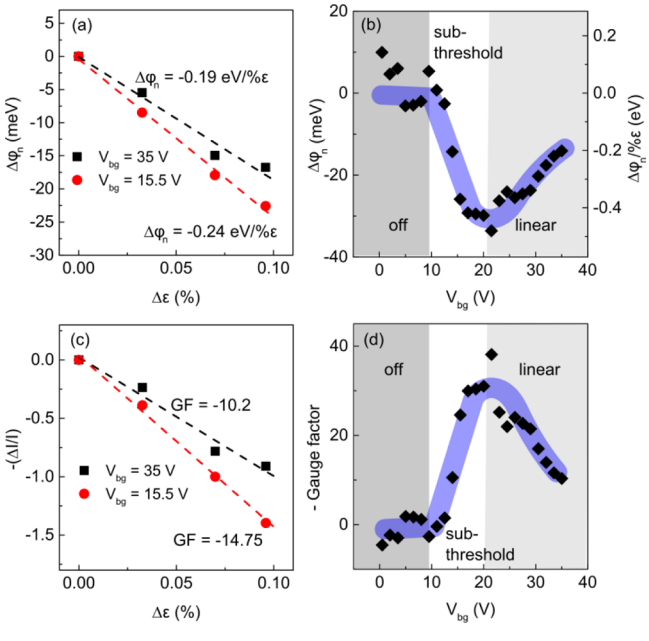

Figure 6. Change of the Fermi level relative to the conduction band edge ($\Delta\varphi_n$) and the gauge factor (GF) were estimated from electrical measurements. (a) The plots of strain dependence of $\Delta\varphi_n$ at different back-gate voltages. The right vertical axis is scaled to $\Delta\varphi_n$ per percent strain applied. (b) The relationship between $\Delta\varphi_n$ and V_{bg} of a representative device. (c) The plots of the strain dependence of $-(\Delta I)/I$ at different back-gate voltages. The slope of the linear fit in (c) is the gauge factor (GF) by definition. (d) The relationship between the GF and V_{bg} of the same device as shown in (b). Similar back-gate dependence is observed for both (b) and (d), and both (a) and (c) show a linear relationship with increasing strain. The solid bands in (b) and (d) are guides to the eye.

To compare the sensitivity of the presented MoS_2 strain sensors with conventional silicon-based devices, one can estimate a commonly used figure of merit of a piezoresistive strain sensor, the so-called gauge factor (GF).[32] The GF is defined as the normalized resistance change per unit strain, GF = $(\Delta R)/R\varepsilon$, where ΔR is the change in resistance compared to that of the unstrained device, R is the resistance of the unstrained device, and ε is the applied strain. Because the FET is operated in the "on" state, the GF can also be defined as GF = $-(\Delta I)/I\varepsilon$, where ΔI is the current change due to strain and I is the current of the unstrained device. The GF is negative for n-type materials (such as the MoS_2 used here) because the resistance decreases with increasing strain, leading to $\Delta R < 0$ ($\Delta I > 0$).[33] Figure 6c shows the $-(\Delta I)/I$ versus $\Delta\varepsilon$ relationship (GF) at selected V_{bg} values. The GF versus V_{bg} relationship is plotted in Figure 6d. Consistent with the back-gate dependence of $\Delta\varphi_n$, this definition leads to a gate-dependent gauge factor in transistor-based devices, with the highest values in the subthreshold regime,[34,35] where an exponential dependence of I_d on V_{bg} occurs and the changes ΔI and Δn are large. A similar nonmonotonic behavior has also been reported in carbon-nanotube-based devices.[36] Because the GF is derived from I_d, the aforementioned mechanism that relates to the gate voltage dependence of $\Delta\varphi_n$ is also applicable to GF. Indeed, if we estimate the magnitude of the gauge factor (Figure 6d), it has the same pronounced gate dependence. The GF is close to 0 if the transistor is switched off (V_{bg} < 10 V) and reaches a maximum of approximately −40 in the subthreshold regime (around V_{bg} = 20 V) before decreasing again in the transition region to the linear regime (V_{bg} > 20 V). This observed nonmonotonic shape can be explained by the combined effect of the band gap change under strain and the Fermi level evolution with changing V_{bg}. This magnitude of GF compares well with that of polycrystalline n-type silicon (−30),[33] although it is lower than that of single crystal silicon (−125).[33] Note that the MoS_2 material used here is polycrystalline; larger GF values may occur in single-crystal MoS_2. Further work is needed to investigate the influence of MoS_2 crystallinity and crystallographic orientation on the gauge factor as well as the electrical response of the device.

Wu et al. previously observed piezoelectricity in two-terminal ungated MoS_2 devices with an odd number of MoS_2 layers.[19] However, piezoelectricity can only occur when large Schottky

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barriers are formed between the source-drain metal contacts and the MoS_2 due to an asymmetric modulation of the two Schottky barriers by strain-induced charges. In our experiments, three-terminal field-effect transistors are used, and the Schottky barriers are lowered significantly by the applied gate bias because the MoS_2 under the contacts is also modulated by the gate biasing.[26,37,38] Therefore, the piezoresistive band gap change dominates the piezoelectric effects.

3. CONCLUSIONS

In conclusion, we have demonstrated piezoresistive strain sensors based on flexible MoS_2 field-effect transistors made from a highly uniform large-area trilayer film. The origin of the piezoresistive effect in MoS_2 is explained to be a strain-induced band gap change, as confirmed by optical spectroscopy. The results are in good agreement with recently reported simulations and spectroscopic studies on strained exfoliated MoS_2. In addition, the strain sensitivity can be tuned by over 1 order of magnitude by modulating the MoS_2 Fermi level with an applied gate bias. The gate-tunable gauge factors can be as high as −40, comparable to that of polycrystalline silicon but for a much thinner active layer (approximately 2 nm).[33] For practical sensing applications, the gate-tunable piezoresistivity is a useful property of transistor-based devices because the relative sensitivity to strain can be adjusted by changing the gate bias.[35]

4. EXPERIMENTAL SECTION

Fabrication of MoS_2 FETs. First, a 265 nm thick SiO_2 layer was grown via thermal oxidation on a heavily phosphorus-doped Si wafer (⟨100⟩, 0.01−0.05 Ohm cm). MoS_2 was synthesized by sulfurizing an electron-beam-evaporated 1 nm thick Mo film on a SiO_2−Si wafer at 1050 °C. A more detailed description of the MoS_2 synthesis and characterization is presented elsewhere.[26] The MoS_2 FETs were fabricated using a two-step standard photolithography process. As a first step, 60 nm thick gold source and drain contacts were deposited by electron beam evaporation in a lift-off process using a positive photoresist (Shipley Microposit S1813). Second, the transistor channels were defined by the photoresist, and the pattern was transferred to MoS_2 by reactive ion etching in a gas mixture of SF_6 and O_2.

Transfer of MoS_2 FETs. The fabrication of flexible devices using a device transfer technique is schematically shown in Figure 1. The as-fabricated MoS_2 FETs were first coated with a thin layer of poly(methyl methacrylate) (PMMA), followed by drying at room temperature (Figure 1a). The PMMA-coated sample was then immersed in buffer oxide etch (BOE, 40% NH_4F/49% HF, 6:1 v/v in water) for 1 day to remove the underlying SiO_2. The released FETs from the substrate were held together by the PMMA supporting layer and floated on the acid bath (Figure 1b). The floating devices were then transferred to a deionized water bath and transferred (fished) (Figure 1c) onto a flexible Al_2O_3−ITO−PET substrate (Figure 1d) (Al_2O_3, 80nm; 17 Ω/□ ITO on a 100 μm thick PET substrate, Solaronix). The 80 nm thick Al_2O_3 gate dielectric was deposited with atomic layer deposition (ALD) at 100 °C. Subsequently, the sample was heated on a hot plate at 150 °C for 5 min, and the PMMA layer was removed by soaking the sample in an acetone bath for 3 h (Figure 1e).

Reflection Spectroscopy. A halogen lamp was used as the broad band light source. The light was focused on the MoS_2 sample using a 50× objective lens, resulting in a spot size of 5−6 μm. Reflected light from the sample was collected using another 50× lens in a backscattering configuration and was sent to a single-pass spectrometer. Two polarizers were inserted before and after the sample to maximize the intensity at the spectrometer. To cancel out the effects of the optical elements and the substrate on the reflection spectra, we measured a reference spectrum (on the substrate away from the MoS_2 film) and then subtracted it from the MoS_2 spectra. The signal was detected with a typical integration time of 3 s.

Electrical Characterization. The electrical measurements were performed using a Keithley 4200-SCS parameter analyzer at room temperature. The drain current at a constant drain-source voltage, V_{ds} = 10 V, was measured versus the applied back-gate voltage sweeping bidirectionally from 0 to 200 V for devices on SiO_2−Si and from 0 to 35 V for devices on the Al_2O_3−ITO−PET substrate. The threshold voltage is defined as the applied back-gate voltage V_{bg} where the drain current I_d equals 10^{-10} A, i.e., the intersection between the transfer curve and the horizontal dashed line in Figure 3b. The current on/off ratio is defined as the ratio of the maximum and the minimum current in the measured gate voltage range. The bending tests were performed sequentially by bending the samples along the longitudinal direction of the MoS_2 channels using substrates with defined radii (R = 7, 2.5, and 0.9 cm). After bending the samples, we measured the devices in the flat state in a high-vacuum (approximately 10^{-5} Torr) chamber to avoid environmental contamination. To test the device performance under strain, we taped the sample on curved (cylindrical) surfaces with different well-defined radii. Each curvature corresponds to a different strain value. The transfer curves of both unstrained and strained devices were recorded.

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Notes

The authors declare no competing financial interest.

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